



CICore Family

SS-CIMAX-V1.0

Spec. Sheet of **CICore1.0** Family

Common Interface Controller for STB

V1.0

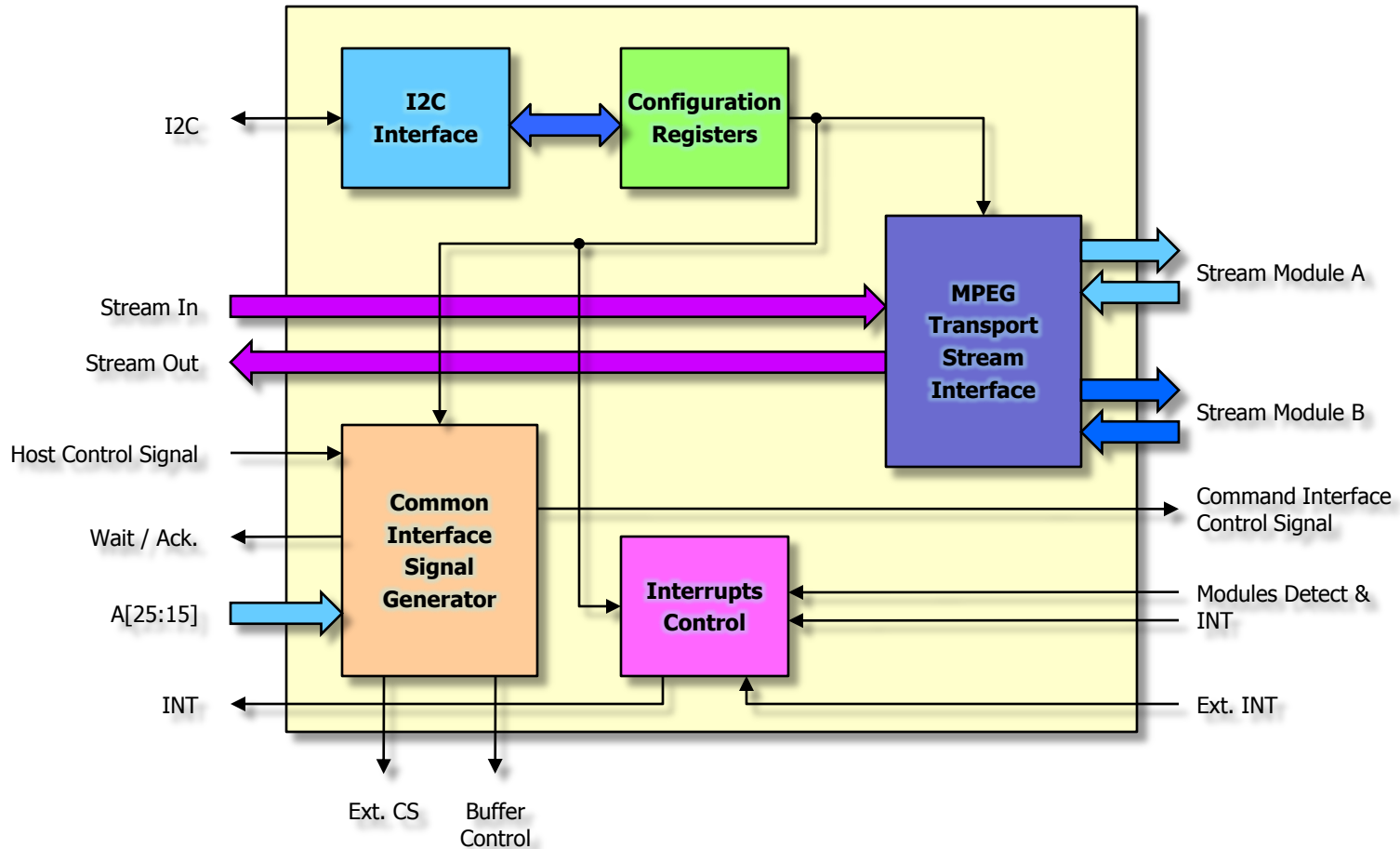
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1. What is CICore

- ◆ CICore1.0 is the common interface controller for digital video receiver and digital TV to adopt the common interface standard (CENELEC EN-50221).
- ◆ CICore1.0 enables the receiver's microprocessor to read the status of the common interface modules and configure the modules such that the modules process the MPEG video stream.
- ◆ CICore1.0 generates the common interface control signals from the commands of the microprocessor.
- ◆ CICore1.0 also supports 8-bit memory card in PC Card Standard for the purpose of memory extension of receiver.
- ◆ CICore1.0 controls the two modules independently and supports hot-plugging of them.
- ◆ CICore1.0 is initialized by I2C bus during start-up.
- ◆ **CICore1.0 is pin compatible with CIMAX device of SCM/ATMEL .**

2. Block Diagram



3. Features

- ◆ Host Interface
 - ✓ I2C for chipset configuration
 - MPEG video stream interface
 - CI/PC Card Module interface
 - ✓ Configurable microprocessor interface
 - ✓ Configurable chip-select and interrupt
- ◆ MPEG Video Stream Interface
 - ✓ MPEG II transport stream compliant
 - ✓ Stream MUX/DEMUX capability
- ◆ Module Interface
 - ✓ CI (Common interface) standard compliant
 - DVB CI (CENELEC EN-50221)
 - ✓ PC Card standard compliant
 - 8-bit data access
 - 26-bit address memory card
 - ✓ Hot plugging capability
 - ✓ Polling and interrupt modes
 - ✓ Two independent module interface
 - ✓ Separate module power control
- ◆ Electrical Specification
 - ✓ 3.3V Voltage Source for Core and I/O
 - ✓ CMOS/LVTTL drive level for all I/O buffers
 - ✓ All input and bi-directional buffers are 5.0V tolerant
- ◆ Package
 - ✓ 128 Pins PQFP

5. Pin Descriptions (1/3)

Pin No.	Name	I/O	Type	Description
1	MDOA[0]	I	CMOS Down	MPEG Data Input from Module A
2	MDOB[1]	I	CMOS Down	MPEG Data Input from Module B
3	MDOA[1]	I	CMOS Down	MPEG Data Input from Module A
4	MDOB[2]	I	CMOS Down	MPEG Data Input from Module B
5	MDOA[2]	I	CMOS Down	MPEG Data Input from Module A
6	CD2B	I	CMOS Up	Card Detect Signal 2 of Module B
7	CD2A	I	CMOS Up	Card Detect Signal 2 of Module A
8	GND		Power	
9	GND		Power	
10	N.C.			
11	N.C.			
12	EXTINT	I	CMOS	Interrupt Signal or External Device
13	EXTCS	O	CMOS TS	Chip Select Signal or External Device
14	INT	O	CMOS TS	Interrupt Output to Microprocessor
15	WAIT/ACK	O	CMOS TS	Wait or Acknowledgement Signal to Microprocessor
16	WR/STR	I	CMOS	Write or Strobe Signal from Microprocessor
17	RD/DIR	I	CMOS	Read or Direction Signal from Microprocessor
18	CS	I	CMOS	Chip Select Signal from Microprocessor
19	A[15]	I	CMOS	Address Output Bit 15 of Microprocessor
20	A[16]	I	CMOS	Address Output Bit 16 of Microprocessor
21	A[17]	I	CMOS	Address Output Bit 17 of Microprocessor
22	A[18]	I	CMOS	Address Output Bit 18 of Microprocessor
23	A[19]	I	CMOS	Address Output Bit 19 of Microprocessor
24	A[20]	I	CMOS	Address Output Bit 20 of Microprocessor
25	A[21]	I	CMOS	Address Output Bit 21 of Microprocessor
26	A[22]	I	CMOS	Address Output Bit 22 of Microprocessor
27	A[23]	I	CMOS	Address Output Bit 23 of Microprocessor
28	A[24]	I	CMOS	Address Output Bit 24 of Microprocessor
29	A[25]	I	CMOS	Address Output Bit 25 of Microprocessor

Pin No.	Name	I/O	Type	Description
30	SDA	I/O	TTL	I2C Data
31	SCL	I	TTL	I2C Clock
32	SA[0]	I	CMOS	I2C Address Bit 0
33	SA[1]	I	CMOS	I2C Address Bit 1
34	RESET	I	CMOS	Chip Reset – High Active
35	CLK	I	CMOS	Clock Input – 27MHz
36	VDD		Power	
37	GND		Power	
38	VDD		Power	
39	GND		Power	
40	MDI[0]	I	CMOS	MPEG Data Input
41	MDI[1]	I	CMOS	MPEG Data Input
42	MDI[2]	I	CMOS	MPEG Data Input
43	MDI[3]	I	CMOS	MPEG Data Input
44	MDI[4]	I	CMOS	MPEG Data Input
45	MDI[5]	I	CMOS	MPEG Data Input
46	MDI[6]	I	CMOS	MPEG Data Input
47	MDI[7]	I	CMOS	MPEG Data Input
48	MIVAL	I	CMOS	MPEG Data Valid Signal Input
49	MISTR	I	CMOS	MPEG Data Start Signal Input
50	MICLK	I	CMOS	MPEG Clock Signal Input
51	VDD		Power	
52	GND		Power	
53	MDO[0]	O	CMOS	MPEG Data Output
54	MDO[1]	O	CMOS	MPEG Data Output
55	MDO[2]	O	CMOS	MPEG Data Output
56	MDO[3]	O	CMOS	MPEG Data Output
57	MDO[4]	O	CMOS	MPEG Data Output
58	MDO[5]	O	CMOS	MPEG Data Output

Notations : TTL (TTL Level), CMOS (CMOS Level), TS (Tristate), Up (Internal Pull-up), Down (Internal Pull-down)

5. Pin Descriptions (2/3)

Pin No.	Name	I/O	Type	Description
59	MDO[6]	O	CMOS	MPEG Data Output
60	MDO[7]	O	CMOS	MPEG Data Output
61	MOVAL	O	CMOS	MPEG Data Valid Signal Output
62	MOSTRT	O	CMOS	MPEG Data Valid Signal Output
63	MOCLK	O	CMOS	MPEG Clock Signal Output
64	VDD		Power	
65	VDD		Power	
66	ADLE	O	CMOS	External Address Buffer Latch Enable Signal
67	ADOE	O	CMOS	External Address Buffer Output Enable Signal
68	DATDIR	O	CMOS	External Data Buffer Direction
69	DATOE	O	CMOS	External Data Buffer Signal or Modules
70	VCCEN	O	CMOS TS	VCC Switch Control Signal or Modules
71	CD1B	I	CMOS Up	Card Detect Signal 1 of Module B
72	CD1A	I	CMOS Up	Card Detect Signal 1 of Module A
73	MDOB[3]	I	CMOS Down	MPEG Data input from Module B
74	MDOA[3]	I	CMOS Down	MPEG Data input from Module A
75	MDOB[4]	I	CMOS Down	MPEG Data input from Module B
76	MDOA[4]	I	CMOS Down	MPEG Data input from Module A
77	MDOB[5]	I	CMOS Down	MPEG Data input from Module B
78	MDOA[5]	I	CMOS Down	MPEG Data input from Module A
79	MDOB[6]	I	CMOS Down	MPEG Data input from Module B
80	MDOA[6]	I	CMOS Down	MPEG Data input from Module A
81	CE1B	O	CMOS TS	Card Enable Signal 1 of Module B
82	CE1A	O	CMOS TS	Card Enable Signal 1 of Module A
83	MDOB[7]	I	TTL Down	MPEG Data Input from Module B
84	MDOA[7]	I	TTL Down	MPEG Data Input from Module A
85	CE2B	O	CMOS TS	Card Enable Signal 2 of Module B
86	GND		Power	
87	CE2A	O	CMOS TS	Card Enable Signal 2 of Module A

Pin No.	Name	I/O	Type	Description
88	OE	O	CMOS TS	Output Enable Signal to Modules
89	IORD	O	CMOS TS	I/O Read Signal to Modules
90	IOWR	O	CMOS TS	I/O Write Signal to Modules
91	MISTRTB	O	CMOS TS	MPEG Data Start Signal to Module B
92	MISTRTA	O	CMOS TS	MPEG Data Start Signal to Module A
93	MDIB[0]	O	CMOS TS	MPEG Data Output to Module B
94	MDIA[0]	O	CMOS TS	MPEG Data Output to Module A
95	MDIB[1]	O	CMOS TS	MPEG Data Output to Module B
96	MDIA[1]	O	CMOS TS	MPEG Data Output to Module A
97	WE	O	CMOS TS	Write Enable Signal to Modules
98	MDIB[2]	O	CMOS TS	MPEG Data Output to Module B
99	MDIA[2]	O	CMOS TS	MPEG Data Output to Module A
100	RDY/IRQB	I	CMOS	RDY/IRQ Signal from Module B
101	RDY/IRQA	I	CMOS	RDY/IRQ Signal from Module A
102	MDIB[3]	O	CMOS TS	MPEG Data Output to Module B
103	MDIA[3]	O	CMOS TS	MPEG Data Output to Module A
104	MIVALB	O	CMOS TS	MPEG Data Valid Signal to Module B
105	MIVALA	O	CMOS TS	MPEG Data Valid Signal to Module A
106	MDIB[4]	O	CMOS TS	MPEG Data Output to Module B
107	MDIA[4]	O	CMOS TS	MPEG Data Output to Module A
108	MICLKB	O	CMOS TS	MPEG Clock Signal to Module B
109	VDD		Power	
110	MICLKA	O	CMOS TS	MPEG Clock Signal to Module A
111	MDIB[5]	O	CMOS TS	MPEG Data Output to Module B
112	MDIA[5]	O	CMOS TS	MPEG Data Output to Module A
113	MDIB[6]	O	CMOS TS	MPEG Data Output to Module B
114	MDIA[6]	O	CMOS TS	MPEG Data Output to Module A
115	MDIB[7]	O	CMOS TS	MPEG Data Output to Module B
116	MDIA[7]	O	CMOS TS	MPEG Data Output to Module A

Notations : TTL (TTL Level), CMOS (CMOS Level), TS (Tristate), Up (Internal Pull-up), Down (Internal Pull-down)

5. Pin Descriptions (3/3)

Pin No.	Name	I/O	Type	Description
117	MOCLKB	I	CMOS Down	MPEG Clock Signal from Module B
118	MOCLKA	I	CMOS Down	MPEG Clock Signal from Module A
119	RSTB	O	CMOS TS	Reset of Module B
120	RSTA	O	CMOS TS	Reset of Module A
121	WAITB	I	CMOS	WAIT Signal of Module B
122	WAITA	I	CMOS	WAIT Signal of Module A
123	REG	O	CMOS TS	REG Signal to Modules
124	MOVALB	I	CMOS Down	MPEG Data Valid Input from Module B
125	MOVALA	I	CMOS Down	MPEG Data Valid Input from Module A
126	MOSTRTB	I	CMOS Down	MPEG Data Start Input from Module B
127	MOSTRTA	I	CMOS Down	MPEG Data Start Input from Module A
128	MDOB[0]	I	CMOS Down	MPEG Data Input to Module B

Notations : TTL (TTL Level), CMOS (CMOS Level), TS (Tristate), Up (Internal Pull-up), Down (Internal Pull-down)

6. Strong Points

- ◆ Wide range of companion chip selection
 - ✓ Fully configurable microprocessor interface
 - ✓ Fully configurable address or data buffer/latch control

- ◆ Independent control of two modules
 - ✓ Interface configuration
 - ✓ Module power control

